GRAPHICS CARD FOR SMOOTHING THE PLAYING OF VIDEO

DESCRIPTION

Cross Reference To Related Applications

[Para 1] This application claims the benefit of U.S. Provisional Application No. 60/481,801, filed 12/16/2003, and included herein by reference.

Background of Invention

[Para 2] 1. Field of the Invention

[Para 3] The present invention relates to a graphics card, and more particularly, to a graphics card for smoothing the playing of video.

[Para 4] 2. Description of the Prior Art

[Para 5] Please refer to Fig. 1. Fig. 1 is a diagram of a graphics card 100 according to the prior art. The graphics card 100 comprises a decoder 120 having a first clock generator 122. The graphics card 100 further comprises a video capture engine 130, a video process engine 150, a memory 140, a video display engine 160, a video process clock generator 152, a second clock generator 162, a TV encoder 110, a liquid crystal display (LCD) output interface 112, a cathode ray tube (CRT) output interface 114, and a plasma display panel (PDP) output interface 116. In the graphics card 100, the clock sources of the video capture engine 130, the video process engine 150 and the video display engine 160 are different. The first clock generator 122 of

the decoder 120 provides CAPCLK to the video capture engine 130; the video process clock generator 152 provides ECK to video process engine 150; and the second clock generator 162 provides DCK to the video display engine 160. Note that DCK of the video display engine 160 must have the same frequency as CAPCLK of the video capture engine 130, that is to synchronize the signal receiving rates of the video capture engine 130 and the video display engine 160 for avoiding a drop-frame phenomenon when outputting video to a display. The drop-frame phenomenon implies that the playing of video is not smooth. However, the first clock generator 122 and the second clock generator 162 are independent phase locked loops (PLLs). Thus, there can be a problem of frequency difference, wherein the signal receiving rates of the video capture engine 130 and the video display engine 160 are different and the drop-frame phenomenon arises.

[Para 6] For instance, in the ITU-R BT601 standard, the two clock generators 122 and 162 are set to generate clocks of 27 MHz, but the second clock generator 162 generates an output clock based on a reference clock instead of based on an output clock generated by the first clock generator 122. Thus, there is likely to be a frequency difference between the clocks generated by the two generators 122 and 162. Suppose that the clock generated by the first clock generator 122 is 27 MHz while the clock generated by the second clock generator 162 is 26.9 MHz. In this case, due to the frequency difference between the two clocks, the drop-frame phenomenon will arise after a long time, that is the playing of video will gradually become less smooth. On the other hand, if the clock generated by the first clock generator 122 is 27 MHz while the clock generated by the second clock generator 162 is 27.1 MHz, the speed of playing is faster than that of video input into the video capture engine 130. Therefore, the player might have to replay the same frame when the frequency difference between the first clock generator 122 and the second clock generator 162 accumulates to the time of playing one frame. No matter whether the drop-frame or the replaying problem arises, the playing of video is not smooth.

Summary of Invention

[Para 7] It is therefore a primary objective of the claimed invention to provide a graphics card for smoothing the playing of video to solve the above-mentioned problems.

[Para 8] The claimed invention discloses a graphics card for smoothing the playing of video. The graphics card includes a video capture engine for receiving a digital video signal, a memory connected to the video capture engine for storing the digital video signals captured by the video capture engine, a video display engine connected to memory for receiving digital video signals stored in the memory, and a first clock generator connected to the video capture engine and the video display engine for providing the same clock to the video capture engine and the video display engine so as to synchronize the signal receiving rates of the video capture engine and the video display engine.

[Para 9] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[Para 10] Fig. 1 is a diagram of a graphics card according to the prior art.

[Para 11] Fig. 2 is a diagram of a first embodiment of a graphics card according to the present invention.

[Para 12] Fig. 3 is a diagram of a second embodiment of a graphics card according to the present invention.

Detailed Description

[Para 13] Please refer to Fig. 2. Fig. 2 is a diagram of a graphics card 200 according to the present invention. The graphics card 200 comprises a decoder 220 having a first clock generator 222. The graphics card 200 further comprises a video capture engine 230, a video process engine 250, a memory 240, a video display engine 260, a video process clock generator 252, a TV encoder 210, a LCD output interface 212, a CRT output interface 214, and a PDP output interface 216. The decoder 220 transforms a received analog video signal (AVS) into a digital video signal (DVS). The video capture engine 230 is utilized for receiving the DVS from the decoder 220 and storing the DVS in the memory 240. The memory 240 is connected to the video capture engine 230. The video process engine 250 accesses the DVS from the memory 240 to enlarge the video, shrink the video, or perform other video effects on the video based on the DVS, and then generates digital video data (DVD) and stores the DVD in the memory 240. The video display engine 260 reads the DVD from the memory 240 and then outputs the DVD to an output interface, such as the TV encoder 210, the LCD output interface 212, the CRT output interface 214 and the PDP output interface 216. Note that the video data read by the video display engine 260 may be the DVS transmitted from the video capture engine 230 to the memory 240 (without special processing) or the digital video data processed by the video process engine 250.

[Para 14] In the graphics card 200, the first clock generator 222 of the decoder 220 is a phase locked loop (PLL) and is connected to the video capture engine 230 and the video display 260 for providing the same clock DCK to both engines 230 and 260 so as to synchronize the signal receiving rates of the video capture engine 230 and the video display engine 260 to avoid the

drop-frame phenomenon. In addition, the first clock generator 222 is further connected to the decoder 220, the TV encoder 210, and the output interfaces 212, 214, and 216 for providing a clock with the same frequency as CAPCLK of the video capture engine 230 and the video display engine 260 to the TV encoder 210 and the output interfaces 212, 214, and 216.

[Para 15] Note that all units inside the graphics card 200 are not located in the same chip. The decoder 220 is located in a first chip 202; the video capture engine 230, the video process engine 250, the video process clock generator 252, the memory 240 and the video display engine 260 are placed in a second chip 204; and the TV encoder 210 and the output interfaces 212, 214 and 216 are placed in a third chip 206. When the first clock generator 222 in the first chip 202 outputs CAPCLK to the video capture engine 230 and the video display engine 260 in the second chip 204 and outputs CAPCLK to the encoder 210 and the output interfaces 212, 214 and 216 in the third chip 206, since CAPCLK is transmitted from one chip to another chip the actual CAPCLK received by the video display engine 260, encoder 210 and the output interfaces 212, 214 and 216 can suffer jitter. Therefore, when displaying video on a screen, the frame may jitter or other problems may occur. In order to avoid this issue and improve the quality of playing, please refer to Fig. 3. Fig. 3 is a diagram of another embodiment according to the present invention that addresses this issue.

[Para 16] Please refer to Fig. 3. Fig. 3 is a diagram of another embodiment of a graphics card 300. The structure of the graphics card 300 is similar to that of the graphics card 200. The same units are labeled with the same numbers and redundant description of functions is omitted. The graphics card 300 includes a second clock generator 270 and a multiplexer 280, differing from the graphics card 200. The second clock generator 270 is connected to the first clock generator 222 and a second input of the multiplexer 280. The second clock generator 270 is a PLL for generating a DCK with the same frequency as the CAPCLK generated by the first clock generator

222 based on the CAPCLK generated by the first clock generator 222. The output 286 of the multiplexer 280 is connected to the video display engine 260, the encoder 210, the output interfaces 212, 214 and 216 for providing the same clock CAPCLK or DCK. In addition, a first input 282 of the multiplexer 280 is utilized for directly receiving the CAPCLK generated by the first clock generator 222 so as to provide the same clock CAPCLK to the video display engine 260, the encoder 210 and the output interfaces 212, 214 and 216 through the output 286 of the multiplexer 280. This is similar to operation of the graphics card 200, which directly provides the same clock to the video capture engine 230, the video display engine 260, the encoder 210 and the output interfaces 212, 214, and 216. In this embodiment, a user can control a control node 288 of the multiplexer 280 to select for output the CAPCLK generated by the first clock generator 222 or the DCK generated by the second clock generator 270.

[Para 17] As mentioned above, due to jitter occurring when CAPCLK is transmitted from one chip to another chip, the second clock generator 270 is used to generate DCK with the same frequency and based on CAPCLK generated by the first clock generator 222. Such a DCK is steadier and the jitter issue can be resolved. Similarly, when the video capture engine 230 receives CAPCLK from the first chip 202, jitter might arise. However, in the second embodiment of Fig. 3, CAPCLK transmitted to the video capture engine 230 is not regenerated as DCK is regenerated by the second clock generator 270. The reason is that if the clock transmitted to the video capture engine 230 has the same frequency as that of the decoder 220 receiving the video, the video data can be correctly received and stored in the memory 240.

[Para 18] In addition, as mentioned above, all units in the graphics cards 200 and 300 are not placed in the same chip. However, the present invention can combine all units in one chip and use the first embodiment in Fig. 2 to avoid the drop-frame phenomenon found in the prior art. In this case, the second clock generator 270 can be omitted.

[Para 19] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.